**REMARKS:**

In the outstanding Office Action, claims 11-29 were rejected. Claims 19, 28 and 29 have been amended for clarification. Claims 1-10 remain cancelled, and new claim 30 has been added. Thus, claims 11-30 are pending and under consideration. No new matter has been added. The rejections are traversed below.

**REJECTION UNDER 35 U.S.C. §102(e):**

Claims 28 and 29 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,049,860 ('860).

'860 discusses pipeline stalling caused due to data dependency of a store instruction in a floating point pipeline (i.e. stalling caused when data to be stored cannot be prepared because a prior instruction has not been completed) (see, column 1, lines 39-44 and column 3, lines 8-27 of '860).

The present invention is directed to a processor execution pipeline that decodes an instruction in a processing stage into one control signal while decoding all other instructions in the processing stage to another control signal to control pipelining of the instructions through processing stages.

The Examiner compares the '860 method for processing floating point store instructions using corresponding information to form control signals with the present invention. The '860 control unit maintains information about the instructions that exist in each pipeline stage and uses the information to form control signals to a dataflow pipeline (see, column 3, lines 41-44 and 49-52 of '860). Based on the information about each instruction, the '860 method forms corresponding control signals to process the store instructions that exist in each pipeline stage, for example, instructions that are and aren't data dependent on other instructions, instructions that are interlocked with another instruction, etc. Each control stage of '860 contains corresponding control information of the instructions and forms corresponding control signals for the respective instructions based on corresponding control information. This means that '860 is directed to utilization efficiency of the pipeline by forwarding the store instruction to an empty stage or feeding back the data to be stored to a store instruction holding stage when the data dependency of the store instruction is resolved (see, column 4, line 47 through column 5, line 16 of '860).

In contrast, independent claims 28 and 29 recite a processor execution pipeline method including, "decoding a first instruction into a first control signal and decoding all other

instructions into a second control signal" and "decoding a second instruction into a third control signal and decoding all other instructions into a fourth control signal". Further, operations are performed on "a first data when receiving the first control signal" and "a second operation on a second data when receiving the second control signal" via first and second processing units where the method selects an output of the second processing unit or the second data that is output via the first processing unit. This enables a processor execution pipeline method that passes data through the respective processing units at the time corresponding instruction is decoded to the processing unit. Further, unnecessary and redundant stage latching units can be significantly decreased by converting one instruction to another to pass through data, which is to be operated in an operator of a next stage, to the next stage when the data is latched in the pipeline so that pipelines exclusively provided for passing through data are not necessary.

For example, the present invention relatively reduces the amount of hardware and power consumption, especially in the multi-stage pipeline technology utilized in the recently used GHz-class processors (e.g. the hyper pipeline used in the Pentium 4 processor). The '860 reference does not discuss reducing a number of stage latching units in a pipeline. Furthermore, in GHz-class processors, the pipeline stages tend to be more segmented as the operating frequency is increased, thus if the '860 method is to be utilized in the GHz-class processors, the delay caused by the increase in the wiring length for forwarding or feeding back on the LSI chip of the processor causes a bottleneck in increasing the frequency. In contrast, according to the present invention, there are no such problems because forwarding or feeding back between pipeline stages are not required.

Accordingly, the '860 method does not teach or suggest, "decoding a first instruction into a first control signal and decoding all other instructions into a second control signal" and "decoding a second instruction into a third control signal and decoding all other instructions into a fourth control signal", as recited in independent claims 28 and 29.

Therefore, withdrawal of the rejection is respectfully requested.

**REJECTION UNDER 35 U.S.C. §103(a):**

Claims 11-27 are rejected under 35 U.S.C. §103(a) as being taught by '860 in view of Texas Instrument's Semiconductor Service Support (TI reference).

The TI reference defines a decoder as any device which converts information from a digital (coded) form into an analog format that is more readily understood either by a person or an electronic system.

The Examiner acknowledges that the '860 method does not teach a first and second instruction decoding units, and thus relies on the TI reference as teaching the same. The combination of the '860 method and the TI reference results in a system for processing floating point store instructions using information regarding instructions in each floating point pipeline stage to form control signals to control progression of the respective instructions through the stages, where the system has a decoder to convert information into a format readily understood by the system.

In contrast, independent claims 11, 15, 19 and 23 recite, "a first instruction decoding unit that decodes a first instruction into a first control signal and decodes all other instructions... into a second control signal" and "a second instruction decoding unit that decodes a second instruction into a third control signal and decodes all other instructions... into a fourth control signal". The combination of the '860 method and the TI reference does not teach or suggest, "a first instruction decoding unit that decodes a first instruction into a first control signal and decodes all other instructions... into a second control signal" and "a second instruction decoding unit that decodes a second instruction into a third control signal and decodes all other instructions... into a fourth control signal".

Independent claims 11 and 19 also recite, "a second processing unit that performs a second operation on a second data when receiving the third control signal and performs a third operation on the second data when receiving the fourth control signal, where the second data is an output of the first processing unit". The combination of the '860 method and the TI reference does not teach or suggest, "a second processing unit that performs a second operation on a second data when receiving the third control signal and performs a third operation on the second data when receiving the fourth control signal, where the second data is an output of the first processing unit", as recited in independent claims 11 and 19.

It is submitted that the independent claims are patentable over the combination of the '860 method and the TI reference.

For at least the above-mentioned reasons, claims depending from independent claims 11, 15, 19 and 23 are patentably distinguishable over combination of the '860 method and the TI reference. The dependent claims are also independently patentable. For example, as recited in claim 20, "the multiplexer selects an output of the second processing unit when receiving either one of the third or the fourth control signals, and selects the second data when receiving the fifth control signal". The combination of the '860 method and the TI reference method does not teach or suggest, selecting "an output of the second processing unit when receiving either one

of the third or the fourth control signals" and "the second data when receiving the fifth control signal" (claim 20) where a second instruction is decoded into a fourth control signal while "all other instructions" are decoded into a fifth control signal (independent claim 19).

Therefore, withdrawal of the rejection is respectfully requested.

**NEW CLAIM:**

New claim 30 has been added to highlight the present invention including "decoding a first instruction in a first processing stage into a first control signal and decoding all other instructions in the first processing stage into a second control signal, and decoding a second instruction in a second processing stage into a third control signal and all other instructions in the second processing stage into a fourth control signal", where "the first instruction and the second instruction are unrelated to one another".

Further, new claim 30 recites, "executing a first operation on a first data upon receipt of the first control signal and holding a result of the execution of the first operation until receipt of the second control signal" and "executing a second operation on the result of the execution of the first operation when receiving the third control signal and holding a result of the execution of the second operation until receipt of the fourth control signal", where the result of the first operation or the second operation is selected as an output.

The combination of the '860 method and the TI reference does not teach or suggest, decoding one instruction into a first control signal while decoding other instructions in the same processing stage into another control signal.

It is respectfully asserted that new claim 30 is distinguishably patentable over the combination of the '860 method and the TI reference.

**CONCLUSION:**

Accordingly, claims 19, 28 and 29 have been amended for clarification, claims 1-10 remain cancelled, and new claim 30 has been added. Thus, claims 11-30 are pending and under consideration.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with the filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 12/23/4 By: _____

J. Randall Beckers
Registration No. 30, 358

1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501